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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,317	10/27/2003	Luc Wuidart	S1022.81058US00	3581

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WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,317	WUIDART ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/27/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Election

1. Acknowledgment is made of applicant's Election, filed 27 December 2004, electing Group I, claims 1-8. Therefore, claims 9-11 are withdrawn from further consideration, as being drawn to a non-elected invention.

The election requirement is made final.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Abadeer et al. (U.S. Pat. No. 5,418,738).

Abadeer, for example in Fig. 3, discloses a multiple-level memory cell, comprising: a storage element formed of several polysilicon resistors (F1a, F1b and F1c; see also, for example, column 7, lines 10-12) connected in series (column 7, lines 20-22) between two input/output terminals (a top input terminal connected to Vdd for an input current, and an output terminal T for an output voltage); and a load (including QFd; see also, for example, column 7, lines 18-20) in series with said resistive element, the junction point (terminal T) thereof forming a read terminal of the memory cell (see Figs. 1A and 1B wherein the cell is read via T), and the respective junctions between said resistors of the storage element being accessible (via QFb and

QFa in Fig. 3); wherein at least certain points among said junctions of the storage element (for example, between F1b and F1c) and the junction of this element with the load (the junction T), are connectable, individually by a switch (QFb or QFc, respectively), either to one of said input/output terminals of the storage element (the top terminal, which is connected to Vdd, via QFb), or to a terminal of application of a predetermined voltage (GND via QFc); wherein the ends of a same resistor are not connectable to the same terminal (see Fig. 3); wherein all polysilicon resistors have identical nominal values (see for example column 7, lines 10-12); wherein the number of possible programmable levels corresponds, at most, to the number of polysilicon resistors of the storage element plus one (for example, for three resistors in Fig. 3, four levels corresponding to one, two, three or no resistors having a low resistance value); wherein the programming is performed by imposing, in one or several of said polysilicon resistors of the storage element, a constraint current greater than a current for which the value of this resistance exhibits a maximum (see for example column 4, lines 14-17 and 43-48 and column 7, lines 30-34 which implies that a programming current is greater than a threshold current, resulting in a reduced resistance value); wherein said constraint current is beyond a read operating current range of the storage element (see for example column 7, lines 18-25 which implies that a read operating current or a sensing current is less than the threshold current).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abadeer et al. (U.S. Pat. No. 5,418,738).

Abadeer discloses a memory cell as in claim 2 above, with the exception of said switches comprising MOS transistors distributed half and half between P-channel transistors and N-channel transistors. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the memory cell of Abadeer by adding one or more resistive elements (similar to F1a, F1b or F1c), along with corresponding programming switches (similar to QFa and QFb), thus resulting in an equal number of P- and N-channel transistors as more resistive elements and programming switches are added, for the purpose of providing a greater programming flexibility for the memory cell (since the additional resistive elements provide additional memory states within the memory cell).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800